Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An apparatus arranged to accept digital data as an input and to process the data according to one of either the Secure Hash Algorithm (SHA-1) or Message Digest (MD5) algorithm to produce a fixed length output word, the apparatus comprising:

a plurality of rotational registers coupled to a read bus to receive and store data, one of said rotational registers arranged to receive the input data;

data stores coupled to the read bus for initialization of some of said plurality of rotational registers according to whether the SHA-1 or MD5 algorithm is used, said data stores including fixed data relating to SHA-1 and MD5 operation;

a plurality of dedicated combinatorial logic circuits having inputs coupled to the read bus and outputs coupled to ~~the~~ a write bus and arranged to perform logic operations on data stored in selected ones of said plurality of registers and to output to the write bus;

a plurality of temporary data storage registers having inputs coupled to the write bus and outputs coupled to the read bus, an output of one of the temporary data storage registers comprising an output of the apparatus for the fixed length output word; and

a control circuit arranged to combine a master clock signal and a control signal and to generate individually gated clock signals only for each active register.

2. (Previously Presented) The apparatus of claim 1 wherein the register arranged to receive the input data is arranged to receive said input data serially.

3. (Previously Presented) The apparatus of claim 1 wherein the registers and combinatorial logic circuits are interconnected for communication via the read and write data busses.

4. (Previously Presented) The apparatus of claim 3 wherein the registers and combinatorial logic circuits are connected to write to a respective bus via respective tristate buffers.

5. (Canceled)

6. (Currently Amended) The apparatus of claim ~~5~~1 wherein said control circuit is further arranged to generate individual enabling signals to control the tristate buffers.

7. (Previously Presented) The apparatus of claim 1 wherein the rotational registers are arranged to be multiplexed prior to connection to a tristate buffer.

8. (Previously Presented) The apparatus of claim 1 wherein the combinatorial logic circuits include a copy circuit, a shift left circuit, a NOT circuit, an ADD circuit, an OR circuit, an AND circuit and an XOR circuit.

9. (Previously Presented) The apparatus of claim 1 wherein the apparatus is implemented as an integrated circuit.

10. (Previously Presented) The apparatus of claim 1 wherein the apparatus further includes circuitry arranged to perform digital signature creation or authentication.

11. (Previously Presented) A circuit, comprising:

a plurality of data storage registers coupled to a read bus to receive and store data to be processed;

a plurality of shift registers for temporary data storage and having inputs coupled to a write bus and outputs coupled to the read bus, an output of one of the shift registers comprising an output of the circuit;

a plurality of logic circuits having inputs coupled to the read bus and outputs coupled to the write bus and for performing operations on data and to output to the write bus; and

a control circuit configured to control the data storage registers, the shift registers, and the logic circuits to selectively perform MD5 and SHA-1 operations on data, the control circuit arranged to combine a master clock signal and a control signal and to generate individually gated clock signals only for each active data storage register.

12. (Previously Presented) The circuit of claim 11, further comprising a plurality of initialization storage registers coupled to the read bus and adapted to store and output initialization data for the MD5 and SHA-1 operations.

13. (Previously Presented) The circuit of claim 12 wherein the read bus and the write bus are selectively coupleable to the plurality of data storage registers, the plurality of shift registers, and the plurality of logic circuits by the control circuit.

14. (Previously Presented) The circuit of claim 11, further comprising a multiplexer to multiplex outputs of the plurality of shift registers to the read bus.

15. (Currently Amended) A circuit, comprising:

circuitry for storing data coupled to a read bus to receive and store data to be processed;

circuitry for temporarily storing the data to be processed and having inputs coupled to a write bus and outputs coupled to the read bus, an output of one of ~~the~~ a plurality of shift registers in the circuitry comprising an output of the circuit;

circuitry for performing combinatorial logic operations having inputs coupled to the read bus and outputs coupled to the write bus and arranged to perform logic operations on the data and output results to the write bus; and

circuitry for controlling coupling of the data storage circuitry, the temporary data storage circuitry, and the circuitry for performing combinatorial logic operations to the read and

write busses to selectively perform MD5 and SHA-1 operations on the data, the controlling circuitry comprising a control circuit arranged to combine a master clock signal and a control signal and to generate individually gated clock signals only for each active data storage circuitry, temporary data storage circuitry, and the shift registers ~~register~~.

16. (Previously Presented) The circuit of claim 15, further comprising circuitry for storing data coupled to the read bus, the data used to initialize the circuit to perform MD5 and SHA-1 operations in response to commands from the control means.

17. (Previously Presented) The circuit of claim 15, further comprising circuitry for multiplexing outputs from the temporary data storage registers to the read bus in response to commands from the control means.

18. (Previously Presented) The circuit of claim 17 wherein the temporary data storage circuitry is configured to receive a stream of data, and the circuit generates on the output data of a fixed length.

19. (Previously Presented) A dual hash algorithm circuit, comprising:

a first bank and a second bank of data storage registers having inputs coupled to a write bus and outputs coupled to a read bus;

a first bank and a second bank of circular shift registers coupled to a read bus to receive and store data, including at least one register to receive a data stream as input to the circuit;

a bank of initialization data registers coupled to the read bus;

a bank of temporary data registers coupled to the read bus;

a plurality of combinatorial logic circuits having inputs coupled to the read bus and outputs coupled to the write bus; and

a control system for selectively coupling and uncoupling the first bank and second bank of data storage registers, the first bank and second bank of circular shift registers, the bank of initialization data registers, the bank of temporary data registers, and the plurality of

combinatorial logic circuits to the respective read bus and the write bus to selectively perform MD5 and SHA-1 operations on the data and to output data of a fixed length in accordance with the selected MD5 and SHA-1 operations, the control system comprising a control circuit arranged to combine a master clock signal and a control signal and to generate individually gated clock signals only for each active temporary data register, initialization register, and the first and second banks of circular shift registers and data storage registers.

20. (Previously Presented) The circuit of claim 19 wherein the control system comprises tristate buffers coupled to the control circuit to couple and uncouple the first bank and second bank of data storage registers, the first bank and second bank of circular shift registers, the bank of initialization data registers, the bank of temporary data registers, and the plurality of combinatorial logic circuits to the respective read and write busses in response to the control circuit.

21. (Previously Presented) The circuit of claim 19, further comprising a multiplexer configured to multiplex outputs from the first bank and second bank of circular shift registers to the read bus.